

## APPENDIX B

The “marked-up” version of the amended claims is as follows:

1. (Amended) A [thin film transistor array substrate for a] liquid crystal display, [the thin film transistor array substrate] comprising:

a plurality of gate lines formed [at] on a [transparent insulating] substrate;

a plurality of data lines [insulatively] insulated from and crossing over [the] said plurality of gate lines [to define pixel regions];

a plurality of pixel regions defined by the crossing of said plurality of gate lines and said plurality of data lines;

a common [electrodes at the] electrode formed in each pixel [regions] region;

a pixel [electrodes at the] electrode formed in each pixel region, spaced apart from [the] said common [electrodes] electrode with a predetermined distance therebetween;

a thin film [transistors] transistor provided to each pixel region[, each of which has] and including a semiconductor pattern; and

a light interception pattern formed of the same material as the semiconductor pattern.

2. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 1, wherein [the] said light interception pattern and [is overlapped with the corresponding] said data line corresponding thereto overlap each other, and said light interception pattern and said [the] common electrode or [the] said pixel electrode close to [the corresponding] said data line corresponding thereto overlap each other.

3. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 1, wherein [the] said light interception pattern [is overlapped with the] and a common electrode or [the] a pixel electrode of [the] a neighboring pixel [regions] region overlap each other.

4. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 1, wherein the semiconductor pattern is connected to [the] said [corresponding] light interception pattern corresponding thereto.

5. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 1, wherein the semiconductor pattern is extended to [the bottom of the corresponding] said data line corresponding thereto.

6. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 1, wherein the light interception pattern is extended [external to the] beyond a periphery of said [the corresponding] data line corresponding thereto.

7. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 1, wherein [the] said common [electrodes are] electrode is formed [at] on the same plane as [the] said plurality of gate lines.

8. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 1, wherein [the] said pixel [electrodes are] electrode is formed [at] on the same plane as [the] said plurality of data lines.

9. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 1, wherein [the] said pixel [electrodes are] electrode is formed [at] on the plane different from [the] said plurality of data lines.

10. (Amended) A [thin film transistor array substrate for a] liquid crystal display, comprising:

an insulating substrate;

a gate line assembly formed on [the] said substrate and comprising a plurality of gate lines, and a plurality of gate electrodes connected to the gate lines;

a [linear] common electrode formed on the substrate and separated from said gate line assembly;

a gate insulating layer covering said gate line assembly and said common electrode;

a semiconductor pattern formed on the gate insulating layer over the gate electrodes;

a light interception pattern formed on the gate insulating layer and formed of the same material as [the] said semiconductor pattern;

a data line assembly comprising:

a source electrode and a drain electrode formed on [the] said semiconductor pattern, and

a plurality of data lines connected to the source electrode and crossing over [the]  
said plurality of gate lines to define a pixel region; and  
a [linear] pixel electrode formed [at] in the pixel region and alternatively located side by  
side with the common electrode, wherein the pixel electrode is coupled to the drain electrode.

11. (Amended) The [thin film transistor array substrate] liquid crystal display of  
claim 10, wherein [the] said light interception pattern [is overlapped with the corresponding] and  
the data line corresponding thereto overlap each other, and said light interception pattern and the  
common electrode or the pixel electrode close to the [corresponding] data line corresponding  
thereto overlap each other.

12. (Amended) The [thin film transistor array substrate] liquid crystal display of  
claim 10, wherein [the] said light interception pattern [is overlapped with the] and said common  
electrode or [the] said pixel electrode of [the] a neighboring pixel [regions] region overlap each  
other.

13. (Amended) The [thin film transistor array substrate] liquid crystal display of  
claim 10, wherein [the] said semiconductor pattern is connected to [the corresponding] said light  
interception pattern corresponding thereto.

14. (Amended) The [thin film transistor array substrate] liquid crystal display of  
claim 13, wherein the semiconductor pattern is extended to [the bottom of the corresponding] the  
data line corresponding thereto.

15. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 14, wherein [the] said light interception pattern is extended [external to the] beyond a periphery of the data line corresponding thereto.

16. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 14, wherein [the] said semiconductor pattern has the same shape as the data line except for [the] a channel portion between the source electrode and the drain electrode.

17. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 10, wherein [the] said pixel [electrodes are] electrode is formed [at] on the same plane as the plurality of data lines.

18. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 17, wherein [the] said semiconductor [patterns are] pattern is extended to [the bottom of the] said pixel [electrodes] electrode.

19. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 10, further comprising a protective layer covering [the] said data line assembly and having a contact [holes] hole, wherein [the] said pixel electrode is formed on the protective layer and connected to the drain electrode through the contact [holes] hole.

20. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 10, further comprising an ohmic contact pattern interposed between [the] said semiconductor pattern and [the] said data line assembly.

21. (Amended) The [thin film transistor array substrate] liquid crystal display of claim 20, wherein the ohmic contact pattern has the same shape as the plurality of data lines.

22. (Amended) A method for fabricating a [thin film transistor array substrate for a] liquid crystal display, comprising the steps of:

forming a gate line assembly and a common line assembly on an insulating substrate, the gate line assembly comprising gate lines and gate electrodes, and the common line assembly comprising common electrodes;

forming a gate insulating layer on the substrate covering the gate line assembly and the common line assembly;

forming a semiconductor pattern [on the gate insulating layer; forming a on the gate insulating layer] and a light interception pattern, both formed of the same material, on the gate insulating layer [of same material as the semiconductor pattern];

forming [on the gate insulating layer] a data line assembly on the gate insulating layer, the data line assembly comprising a source electrode and drain electrode, and a plurality of data lines; and

forming a pixel electrode.

23. (Amended) The method of claim 22, wherein the data line assembly is formed [at] on the same plane as the pixel electrodes.

24. (Amended) The method of claim 23, wherein the light interception pattern, the semiconductor pattern, the data line assembly and the pixel electrode are [formed through photolithography using a] patterned by photoresist [pattern] patterns.

25. (Amended) The method of claim 24, wherein the photoresist patterns comprise:  
a first pattern with a predetermined thickness placed at [the] a channel portion between the source and the drain electrodes as well as at the light interception [patterns] pattern,  
a second pattern having a thickness larger than the thickness of the first pattern, and  
a third pattern having a thickness smaller than the thickness of the first pattern.

26. (Amended) The method of claim 25, wherein the photoresist patterns are formed [using one] by a single mask.

27. (Amended) The method of claim 26, wherein [the] said steps of forming the semiconductor pattern, the light interception pattern, the data line assembly and the pixel electrode, further comprise the steps of:

sequentially depositing a semiconductor layer and a conductive layer on the gate insulating layer;

coating a photoresist film onto the conductive layer;

exposing the photoresist film to light through the mask;

developing the photoresist film to form the photoresist patterns, the second photoresist pattern being placed over the data line assembly;

etching the conductive layer under the third photoresist pattern and the underlying semiconductor layer to [from] form the semiconductor pattern and the light interception pattern;

removing the first photoresist pattern through ashing;

etching the conductive layer the second photoresist pattern as mask to complete the data line assembly and the pixel electrodes; and

removing the remaining photoresist pattern.

28. (Amended) The method of claim 27, wherein the semiconductor pattern has the same shape as the data line assembly except for the channel portion between the source electrode and the drain electrode.

29. (Amended) The method of claim 28, wherein the light interception pattern, the semiconductor pattern and the data line assembly are formed [through photolithography using] by a photoresist pattern.

30. (Amended) The method of claim 29, wherein the photoresist pattern comprises:  
a first pattern with a predetermined thickness placed at the channel portion between the source electrode and the drain electrode,

a second pattern having a thickness larger than the thickness of the first pattern, and

a third pattern having a thickness smaller than the thickness of the first pattern.



31. (Amended) The method of claim 30, wherein the photoresist pattern is formed [using one] by a single mask.

32. (Amended) The method of claim 31, wherein [the] said step of forming the semiconductor pattern, the light interception pattern, and the data line assembly further comprises steps of:

sequentially depositing a semiconductor layer and a conductive layer on the gate insulating layer;

coating a photoresist film onto the conductive layer;

exposing the photoresist film to light through the mask;

developing the photoresist film to photoresist patterns, the second photoresist pattern being placed over the data line assembly;

etching the conductive layer under the third photoresist pattern and the underlying semiconductor layer to form the semiconductor patterns and the light interception patterns;

removing the first photoresist pattern through etch back, and etching the second photoresist pattern;

etching the conductive layer using the second photoresist pattern as mask to complete the data line assembly; and

removing the remaining photoresist pattern.

33. (Amended) The method of claim 32, wherein the pixel [electrode is] electrode is formed [at] on the plane different from the data line assembly.

34. (Amended) The method of claim 33, further comprising the step of:  
forming a protective layer after forming the data line assembly to cover the data line  
assembly; and  
forming the pixel electrodes [being formed] on the protective layer.

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